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SOME QUANTUM LIMITS FOR SCALING OF ELECTRONIC DEVICES – ESTIMATIONS AND MEASUREMENTS

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Abstract

In this paper we discuss some physical limits for scaling of transistors and conducting paths inside of semiconductor integrated circuits (ICs). Since 40 years only a semiconductor technology, mostly the CMOS and the TTL technologies, are used for fabrication of integrated circuits on an industrial scale. Miniaturization of electronic devices in integrated circuits has technological limits and physical limits as well. In 2010 best parameters of commercial ICs shown the Intel Core i5-670 processor manufactured in the technology of 32 nm. Its clock frequency in turbo mode is 3.73 GHz. A forecast of the development of the semiconductor industry (ITRS 2011) predicts that sizes of electronic devices in ICs circuits will be smaller than 10 nm in the next 10 years. At least 5 physical effects should be taken into account if we discuss limits of scaling of integrated circuits.

Keywords: nanostructure, quantum effect, integrated circuits.

1. Introduction

Scaling of electronic devices in integrated circuits has technological limits and physical limits as well. Since 40 years only a semiconductor technology, mostly the CMOS and the TTL technologies, are used for fabrication of integrated circuits on an industrial scale. Probably the CMOS technology will be used at least in the next 10-15 years. Now (2012) good parameters of commercial ICs shows the dual-core Intel Core i5-670 processor manufactured in the technology of 32 nm. Its clock frequency in turbo mode is 3.73 GHz. The other example is the quad-core Intel Core i7-975 manufactured in the technology of 45 nm. The last forecast of the development of the semiconductor industry (the International Technology Roadmap for Semiconductors, ITRS 2011) predicts that sizes of electronic devices in ICs will be smaller than 10 nm in the next 10 years [1]. The physical gate length in a MOSFET will even amount to 6 nm (see Table 1) in the year 2026. One can notice that the forecasts of 2007 (ITRS 2007) gave different values of the predicted length of a physical gate in ICs: 9 nm in 2016 and 4 nm in 2022.

Our analysis of scaling of electron devices is not the first one (e.g. [2]) but we underline different effects than other authors. At least 5 physical effects should be taken into account if we discuss limits of miniaturization of integrated circuits:

- quantization of both electrical and thermal conductance in narrow and thin transistor channels and in conducting paths,
- spread of doping atoms in a semiconductor material; each dopant would induce a relatively high potential bump,
- propagation time of electromagnetic wave along and across a chip (IC),
- electrostatics: loss of electrostatic control of the drain current vs the gate voltage,

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- electron tunneling between the source and the drain inside a MOSFET through an insulation (oxide).

Table 1. Data of integrated circuits (IC) according to the Report of The International Technology Roadmap for Semiconductors (Edition 2011[1]).

Year		2011	2013	2015	2017	2020	2026
Physical gate length in a FET transistor inside of ICs (microprocessor unit – MPU)	nm	24	20	17	14	12.5	5.9
Clock frequency (on chip MPU)	GHz	3.74	4.05	4.38	4.74	5.33	6.74
Functionality of IC (number of transistors)	mln	2212	4424	8848	17696	35391	70782
Supply voltage	V	0.93	0.87	0.81	0.75	0.70	0.54
Dissipated power (cooling on)	W	161	149	143	130	130	?

We discuss the spread of doping atoms in a semiconductor material and quantization of both electrical and thermal conductance in nanostructures. We mention the other physical effects important for scaling of integrated circuits only.

2. Quantization of electrical conductance in nanostructures

Electric and thermal proprieties of electronic devices or paths with nanometric sizes are no more described by the classical theory of conductance but by quantum theories. The theoretical quantum unit of electrical conductance $G_0 = 2e^2/h$ was predicted by Landauer in his theory of electrical conductance [3]. Parameters characterizing the system are the Fermi wavelength – λ_F ($\lambda_F = 2\pi/k_F$, where k_F is the Fermi wave-vector) and a mean free path – Λ. For metals like gold $\lambda_F \approx 0.5$ nm is shorter than the free electron path Λ ($\Lambda_{Au} = 14$ nm). If the length of the system is shorter than the free electron path, the impurity scattering is negligible, so the electron transport is ballistic. If a wire has the cross-section dimensions comparable with the Fermi wavelength – λ_F, and its length L is less than Λ, the system can be regarded as one-dimensional (1-D), the electron – as a wave, and one can expect quantum effects – see Fig. 1.

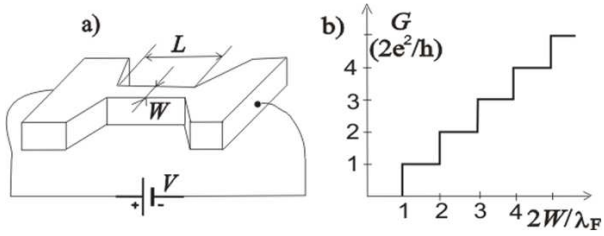

Fig. 1. Conductance quantization in a nanowire (conductor with length $L < \Lambda$ and width W comparable with the length of the Fermi wave λ_F): a) nanowire outline (the third dimension is not considered); b) conductance quantization G versus width W.

Assuming that the wide contacts are infinitely large, the electron movements are in the thermodynamic equilibrium described by Fermi-Dirac statistic. When the electrons enter a 1D conductor, non-equilibrium states occur with negative and positive velocities. If there is a resultant current, the states with positive velocities correspond to high energy [3]. According

to the Büttiker [4] model the hamiltonian of the perfect conductor can be expressed as follows:

$$H = \frac{1}{2m^*}\left(\hbar^2 k_x^2 + \hbar^2 k_y^2\right) + V(x), \tag{1}$$

where y is a dimension along the wire, x is in the transverse direction, m^* is the effective mass of the electron, $V(x)$ denotes the potential well of the width W, k_y is a wavevector along y and k_x is a wavevector along x. Because of the narrowness of the potential wall $V(x)$ the energy for the transverse propagation is quantized:

$$E_{Tj} = \frac{\hbar^2 k_x^2}{2m^*} = \frac{\hbar^2}{2m^*}\left(\frac{j\pi}{W}\right)^2. \tag{2}$$

For the Fermi level $E_F = E_j$ there is a number $N \sim 2W/\lambda_F$ of states E_{Tj} below the Fermi surface. Let us assume that thermal energy k_BT is much smaller than the energy gap between levels, and that both wide contacts are characterized by chemical potentials μ_1 and μ_2. Then current of electrons in j^{th} state is equal to:

$$I_j = ev_j\left(\frac{dn}{dE}\right)_j \Delta\mu, \tag{3}$$

where n is the concentration of the carriers, v_j is the velocity along y and $(dn/dE)_j$ is the density of states at the Fermi level for j^{th} state and $\Delta\mu = \mu_1 - \mu_2$. For a 1D conductor the density of states is

$$\frac{dn}{dk} = \frac{1}{2\pi} \text{ and } \left(\frac{dn}{dE}\right)_j = \left(\frac{dn}{dk}\frac{dk}{dE}\right)_j = \frac{2}{hv_j}. \tag{4}$$

The factor of 2 results from spin degeneracy. Hence, the current for j^{th} state $I_j = \frac{2e^2}{h}V$ does not depend on j (where the electrical potential difference $V = \Delta\mu/e$). Total current $I = \sum_{j=1}^{N} I_j$, hence the conductance is expressed as

$$G = \frac{2e^2}{h}N, \tag{5}$$

where N is the number of transmission channels. For the 1-D system with thickness $H \le \lambda_F$, N depends on the width of the wire, $N = \text{int}(2W/\lambda_F)$. For a 2-D system, with H,

$$W \ge \lambda_F,\ N = \text{int}(W \times H/\lambda_F^2), \tag{6}$$

where int (A) means the integer of A. However, defects, impurities and irregularities of the shape of the conductor can induce scattering, then conductivity is given by the Landauer equation:

$$G = \frac{2e^2}{h}\sum_{i,j=1}^{N} t_{ij}, \tag{7}$$

where t_{ij} denotes probability of the transition from j^{th} to i^{th} state. In the absence of scattering $t_{ij} = \delta_{ij}$ thus Eq. (7) is reduced to Eq. (5). Fig. 1 presents the picture of a path (nanowire) – the

constriction in an electrical conductor with dimension W (width), H (thickness) and L (length).

A set-up for measurements of electrical conductance in nanowires formed by mechanical contact between two microwires is shown in Fig. 2. The experimental setup consisted of a pair of metallic wires (they formed a nanowire), a digital oscilloscope, a motion control system (not shown in the picture) and a PC. Instruments are connected into one system using the IEEE-488 interface. There was a resistor R_p = 1 kΩ in series to the connected wires. The circuit was fed by a constant voltage V_s and measurements of current $I(t)$ have been performed.

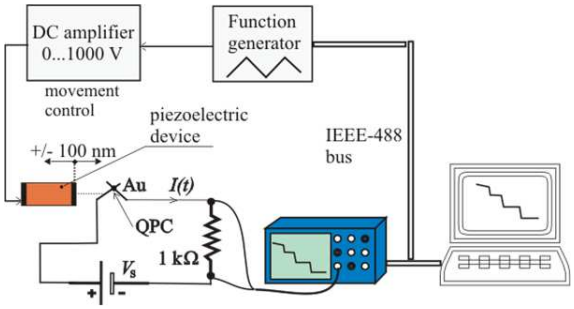

Fig. 2. The measurement system for investigation of electrical conductance in nanowires.

Transient effects of making contact or breaking the contact give a time- dependent current. The voltage V_p on the resistor R_p was measured with a computer-controlled oscilloscope. The piezoelectric device is used to control the backward and forward movement of the macroscopic wires between which nanowires are formed. A high voltage amplifier controlled by a digital function generator supplies the piezoelectric device. Both electrodes (macroscopic wires) are made of a 0.5 mm diameter wire. The conductance was measured between two metallic electrodes, moved to contact by the piezoelectric tube actuator. The oscilloscope was triggered by a single pulse. All experiments were performed at room temperature and at ambient pressure. The quantization of electric conductance depends neither on the kind of element nor on temperature. For conductors and semiconductors the conductance quantization in units of $G_0 = 2e^2/h = (12.9\ \text{k}\Omega)^{-1}$ was measured in many experiments.

The quantization of electric conductance depends neither on the kind of metal nor on temperature. However, the purpose of studying the quantization for different metals was to observe how the metal properties affect the contacts between wires. For nonmagnetic metals, the conductance quantization in units of $G_0 = 2e^2/h = 7.75\times10^{-5}$ [A/V] = $(12.9\ \text{k}\Omega)^{-1}$ was previously observed for the following nanowires: Au-Au, Cu-Cu, Au-Cu, W-W, W-Au, W-Cu [5]. The quantization of conductance in our experiment was evident. All characteristics showed the same steps equal to $2e^2/h$. We observed two phenomena: quantization occurred when breaking the contact between two wires, and quantization occurred when establishing the contact between the wires. The characteristics are only partially reproducible; they differ in number and height of steps, and in the time length. The steps can correspond to 1, 2, 3 or 4 quanta. It should be noted that quantum effects were observed only for some of the characteristics recorded. The conductance quantization has been so far more pronouncedly observed for gold contacts. Fig. 3 shows example plots of conductance vs. time during the process of drawing Au-Au and Cu-Au nanowire, respectively, for the bias voltage V_s = 0.42 V.

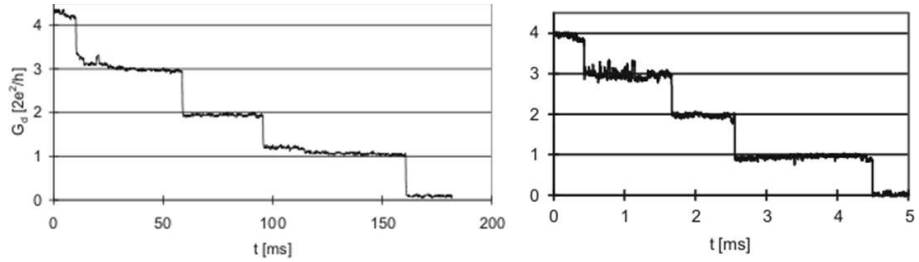

Fig. 3. Conductance quantization in gold nanowires (left) and in gold-copper nanowires (right) at 300 K (measurements were carried out by M. Wawrzyniak).

Let us consider a silicon path with length L = 20 nm ($L < \Lambda_{Si}$), width W = 4 nm, thickness H = 4 nm and λ_F = 1 nm. Such path is a nanowire with the conductance: $G_P = (2e^2/h) \times N$; using (2) N = 16; thus $G_P = 7.75 \times 10^{-5} \times 16 = 12.4 \times 10^{-4}$ [A/V]. The resistance of the path $R_P = 1/G_P$ = 800 Ω, thus it is surprisingly high. The electrical capacity of a meter of the path is 2 pF/cm [5], so for L = 20 nm $C_P = 4 \times 10^{-18}$ F. The path inside an IC forms a low-pass RC filter with the upper frequency $f_u = 1/(2\pi R_P C_P) \approx 50 \times 10^{12}$ Hz. Thus the path-nanowire filters the signals.

3. Quantization of thermal conductance in nanostructures

It is generally known that limits for speed-up of digital circuits, especially microprocessors, are determined by thermal problems. Both electrical G_E and thermal G_T conductance of a nanostructure relate to the same process: electron transport in nanostructures. Therefore there are several analogs between the two physical quantities. Electron transport in a nanowire creates two effects: an electrical current $I = G_E \times \Delta V$ and a heat flux density $Q_D = G_T \times \Delta T$, where G_E – electrical conductance of a sample, ΔV – difference of electrical potentials, G_T – thermal conductance of a sample, ΔT – temperature difference.

$$G_E = \sigma \times A/l, \quad G_T = \lambda \times A/l, \tag{8}$$

where σ – electrical conductivity, λ – thermal conductivity, l – length of a sample (e.g. nanowire), A – area of the cross-section of a sample.

Quantized thermal conductance for ballistic transport of electrons and phonons in one-dimensional systems (e.g. nanowires) was predicted theoretically by Geiner [6] and Rego [7] using the Landauer theory. The thermal conductance is considered in a similar way like the electrical conductance. In one-dimension l systems conductive channels are formed. Each channel contributes to the total thermal conductance with the quantum of thermal conductance G_{T0}. Quantized thermal conductance and its quantum (unit) G_{T0} was confirmed experimentally by Schwab [8]. The quantum G_{T0} of thermal conductance

$$G_{T0}\,[\mathrm{W/K}] = (\pi^2 k_B^2 / 3h)\, T = 9.5 \times 10^{-13} T\,, \tag{9}$$

depends on the temperature (9). At T = 290 K, the value of $G_{T0} = 2.8 \times 10^{-10}$ [W/K]. This value is determined for an ideal ballistic transport (without scattering) in a nanowire, with the transmission coefficient t_{ij} = 100%. It means that in all practical cases (for $t_{ij} < 100\%$) the thermal conductance is below the limit given by formula (9). However an analysis of thermal conductance is more complex than that of electrical conductance because of contribution of either phonons or electrons in heat exchange.

Table 2. Electrical resistance R and thermal conductance G_T of gold nanowire with diameter D (Fermi length λ_F = 0.5 nm).

Diameter D		nm	0.5	1.0	1.5	2.0	2.5	3.0
Number of channels		–	1	4	9	16	25	36
Electrical resistance	$R = 1/G_E$	Ω	12 903	3226	1434	806	516	358
Thermal conductance	G_T (at 300 K)	10^{-9} [W/K]	0.285	1.14	2.56	4.56	7.12	10.26

The thermal conductance of a nanowire is very small. We can compare the thermal conductance in a nanowire with the thermal conductance of Au microwire which connects a silicon part with a metallic terminal (pin) in a transistor. For a microwire with a length of L = 1.5 mm and a diameter D = 25 μm the thermal conductance is much larger: $G_T \approx 10^{-4}$ [W/K]

One can obtain a similar (but not the same) value of the quantum of thermal conductance G_{T0} using the Wiedemann-Franz law. The law describes the relation between the thermal conductivity λ and electrical conductivity σ of a sample for macroscopic objects.

$$\frac{\lambda}{\sigma} = \frac{1}{3}\left(\frac{\pi k_B}{e}\right)^2 T = L \times T = 2.35 \times 10^{-8} T\,, \tag{10}$$

where e – electron charge, k_B – Boltzmann constant, L – Lorenz number, T – temperature.

The Wiedemann-Franz law is valid for the relation between conductances G_T/G_E as well. The value of G_{T0} can be obtained directly from (7).

$$G_{T0} = L \times T \times G_{E0} = \frac{1}{3}\left(\frac{\pi k_B}{e}\right)^2 T \times \frac{2e^2}{h} = \frac{2}{3}\frac{(\pi k_B)^2}{h} \times T = 1.89 \times 10^{-12} T \ \text{[W/K]}. \tag{11}$$

The value of G_{T0} obtained from the Wiedemann-Franz law is twice as large than that from (9) and it is not correct.

A single nanowire should be considered together with its terminals (Fig. 4). They are called reservoirs of electrons. Electron transport in the nanowire is ballistic itself, it means the transport without scattering of electrons and without energy dissipation. The energy dissipation occurs in terminals. Because of the energy dissipation, the local temperature T_{term} in terminals is higher than the temperature T_{wire} of nanowires itself. The heat distribution in terminals of a nanostructure should be analyzed.

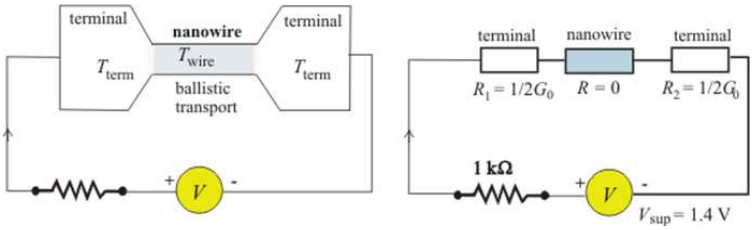

Fig. 4. Conductance distribution in a nanowire with ballistic transport.

In small structures the dissipated energy is quite large. For the first step of conductance quantization, $G_E = G_{E0} = 7.75 \times 10^{-5}$ [A/V], and at the supply voltage V_s = 1.4 V the current in the circuit I = 100 μA (I = 190 μA for the second step of quantization). The power dissipation in terminals of nanowires is $P = I^2/G_{E0}$ = 130 μW for the first step and P = 230 μW for the second step. One ought to notice that the density of electric current in nanowires is extremely high. The diameter of the gold nanowire in the first step of quantization can be estimated to

D = 0.29 nm (the diameter of a gold atom), so for I = 100 μA the current density $J \approx 10^{11}$ [A/cm^2].

4. Spread of doping atoms in a semiconductor material

Classical theories of electrical and thermal conductance assume a huge number of atoms and free electrons. Let us assume a silicon cube with one-side dimension of a and with common doping of 10^{16} cm^{-3}. In a n-doped silicon cube with the size of (100 nm)^3 there are 5×10^7 atoms and 10 free electrons at 300 K, but in the Si cube with the size of (10 nm)^3 there are 5×10^4 atoms and a 1% chance only to find **one** free electron. Free electrons are necessary for electrical conductance as charge carriers. It means not only that classical theories of conductance are not valid for nanostructures. It means that common doping in semiconductor material is not sufficient for electronic devices of nanometer size.

In order to keep the conductive properties of the semiconductor material one should apply more intensive doping, eg. 10^{20} cm^{-3}. However such intensive doping decreases the resistivity of the material dramatically from 2×10^{-3} Ωm to 10^{-5} Ωm, respectively (for n-type Si, at 300 K). The low number of free electrons should be scattered evenly in the whole volume of the material.

5. Other physical limits

The channel length L_E of a Si MOSFET, limited by a degradation of electrostatic control in the transistor, was analyzed by Frank [2] and Likharev [9]. The minimal channel length L_E (see Fig. 5) depends on the thickness of channel H_{ch}, thickness of the insulation layer H_i, dielectric constants of the channel ε and insulation ε_i – formula (8) [8].

$$L_E = \left(\frac{\varepsilon H_{ch} H_i}{2\varepsilon_i} \right)^{1/2}. \tag{12}$$

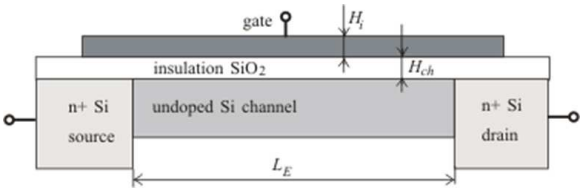

Fig. 5. MOSFET transistor – the simple model.

If we take the ratio $\varepsilon_i/\varepsilon \approx 0.3$ (for silicon oxide and silicon), thickness H_{ch} = 2 nm, H_i = 1.5 nm – the estimated minimal length of the channel is $L_E \approx 3$ nm. The channel length L_E can be shorter if a better insulator than silicon oxide (SiO_2) would be applied. The following materials are tested as an insulator for MOSFETs: silicon nitride, hafnium oxide and zirconium silicate.

The next limit to miniaturization of electronic devices comes from source-to-drain tunneling through the potential barrier along the channel. The tunneling effect depends on the channel length L and the supply voltage. Because of tunneling the minimal channel length for a silicon device is around 2 nm [9].

High-tech microprocessors have dimensions over 30 mm. A new Intel product, the quad-core Intel Core i5-670 has a width a = 37.5 mm and a length b = 37.5 mm. The pins of the IC are distributed on the bottom plate, along its four sides too.

The period of the highest clock frequency of the Intel Core i5-670 (f_{ck} = 3.73 GHz) is T_{ck} = 270 ps. But the propagation time for an electromagnetic wave on the way of (a + b) is:

$T_p = (a + b)/v = 75$ mm/2.5×10^8 m/s = 300 ps (v – speed of an electromagnetic wave in a thin silicon layer). Thus, the propagation time of the clock signal along the IC is longer than the period of the clock signal. In the result different pins of the IC are activated by different pulses of the clock signal.

6. Discussion

Conductance quantization in nanostructures has proved to be observable in a simple experimental setup, giving an opportunity to investigate subtle quantum effects in electrical conductivity. The energy dissipation in nanowires takes part in their terminals. Because of the energy dissipation the local temperature in terminals is higher than the temperature of a nanowire itself.

The operating frequency of a transistor and the clock frequency of an integrated circuit (e.g. microprocessor) can be 100 times higher than 3-6 GHz. A research group from the Georgia Institute of Technology and IBM has demonstrated that the first silicon-germanium transistor was able to operate at frequency above 500 GHz [10]. Though the record performance was attained at low temperature (4.5 K), the results have shown that the upper bound for performance in silicon-germanium devices can be higher than originally expected. An integrated circuit with the mentioned Si-Ge transistors was tested as well. It was a monolithic 5-bit SiGe BiCMOS as the X-ray radar receiver [11].

According to the state of the art the minimal gate length in a MOSFET in silicon integrated circuits is around 3 nm (thus – technology of 3 nm!). However technological limits allow to apply only 10 nm-technology in the next 10 years.

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